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IBM CORP (YA)
C/O YEE & ASSOCIATES PC
P.O. BOX 802333
DALLAS, TX 75380

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/757,212
Filing Date: January 14, 2004
Appellant(s): DEWITT ET AL.

Francis Lammes
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed December 11, 2006 appealing from the Office action mailed September 7, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,549,998	Pekarich et al.	4-2003
5,887,159	Burrows	3-1999
5,797,019	Levine et al.	8-1998
2003/0101367	Bartfai et al.	5-2003

IBM, "Hardware Cycle Based Memory Residency", May 22, 2003, ip.com, IPCOM000012728D, pp. 1-2

Hyde, Randall, "The Art of Assembly Language", 2001, Linux Edition, pp. 247-248

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-2, 4, 8, 9-10, 12, 16-18, 20, and 23 are rejected under 35 U.S.C. 103(a) as being obvious over Pekarich et al. (U.S. Patent 6,549,998) in view of IBM Technical Disclosure, "Hardware Cycle Based Memory Residency," hereafter "IBMTD," and in further view of Burrows (U.S. Patent 5,887,159).

As per claim 1, Pekarich discloses a method in a data processing system for processing instructions, the method comprising:

receiving a threshold value and an identification of a plurality of addresses to be monitored during the execution of a computer program (col. 4, lines 61-63; col. 3, lines 7-12; col. 1, lines 32-42);

Pekarich does not expressly disclose associating hardware counters with the plurality of addresses;

executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered;

and performing an action in response to a determination that a predefined relationship between the threshold value and a combination of values obtained from the hardware counters is present.

IBMTD discloses associating hardware counters with the plurality of addresses (pg. 1, paragraph 3, lines 1-2); *It should be noted that each page is associated with a page frame table which is in turn associated with physical addresses.*

and performing an action in response to a determination that a predefined relationship between the threshold value and a combination of values obtained from the hardware counters is present (pg. 1, paragraph 5, lines 8-10). *It should be noted that "page given immediately to the application requesting it when LRU runs" is analogous to "performing an action", "the difference between the hardware counter and the PFT counter is greater than the threshold" is analogous to "a predefined relationship between the threshold value and a combination of values obtained from the hardware*

counters is present", and "the difference between the hardware counter and the PFT counter" is analogous to "combination of values obtained from the hardware counters."

Pekarich and IBMTD are analogous art because they are from the same field of endeavor, that being memory management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement IBMTD's PFT and hardware counters with Pekarich's address range table.

The motivation for doing so would have been to reduce the expense of operations by allowing more immediate and more cost-effective memory management with the use of a hardware cycle counter and PFT cycle counter (IBMTD, pg. 1, paragraph 4, lines 5-7).

The combination of Pekarich/IBMTD does not expressly disclose executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered.

Burrows discloses executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered (col. 5, lines 13-17 and 31-34; Fig. 5, elements 520 and 540). *It should be noted that the "hit field" is analogous to the "hardware counter", a " "hit" to an entry in the prediction table" is analogous to an "address access", and the "best_hint field" is analogous to the "performance indicator." It should also be noted that the entries in the prediction table*

are associated with instruction addresses (col. 2, lines 2-4). Lastly, it should also be noted that in order for a determination to be made as to whether the current hint field is identical to the best_hint field, it is inherently required the best_hint field is accessed (i.e. encountered).

The combination of Pekarich/IBMTD and Burrows are analogous art because they are from the same field of endeavor, that being data processing systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Burrow's dynamic determination of hint field values within Pekarich/IBMTD's address range table.

The motivation for doing so would have been to measurably improve system performance by making code run faster (Burrows, col. 6, lines 16-20).

Therefore, it would have been obvious to combine Pekarich, IBMTD, and Burrows for the benefit of obtaining the invention as specified in claim 1.

As per claim 2, the combination of Pekarich/IBMTD/Burrows discloses arithmetically combining values of the hardware counters to generate a combined counter value (IBMTD, pg. 1, paragraph 5, line 8); *It should be noted that "the difference between the hardware counter and the PFT counter" is analogous to "arithmetically combining values of the counters to generate a combined value counter value."*

comparing the combined counter value to the threshold value (IBMTD, pg. 1, paragraph 5, lines 8-9);

and performing the action in response to a relationship between the combined counter value and the threshold value being present (IBMTD, pg. 1, paragraph 5, lines 9-10).

As per claim 4, the combination of Pekarich/IBMTD/Burrows discloses the steps of arithmetically combining values of the hardware counters, comparing the combined counter value, and performing the action are performed in response to incrementing a hardware counter (Pekarich, col. 5, lines 17-23). *It should be noted that arithmetically combining values of counters, comparing the combined counter value, and performing the action are all done during separate iterations. The counters must be incremented by either +1 or +2 for the each iteration to occur. Therefore, the counters must first be incremented for the separate actions of arithmetically combining values of counters, comparing the combined counter value, and performing the action to occur.*

As per claim 8, the combination of Pekarich/IBMTD/Burrows discloses arithmetically combining values of the hardware counters includes combining values in accordance with a condition indicated by a performance monitoring application (IBMTD, pg. 1, paragraph 5, line 8); *It should be noted that IBMTD discloses subtracting (i.e. arithmetically combining) values of the "hardware" and "PFT" counters. It is inherently required that this subtraction function of the ALU (i.e. a condition) is indicated by commands from the CPU (i.e. a performance monitoring application).*

As per claim 9, the claim is rejected for the same reasons as cited in claim 1 above combined with Pekarich's disclosure of a computer program product in a computer readable recordable-type medium for processing instructions (Pekarich, Pekarich, col. 5, lines 47-55).

As per claim 10, the claim is rejected for the same reasons as cited in claim 2 above combined with Pekarich's disclosure of a computer program product in a computer readable recordable-type medium for processing instructions (Pekarich, col. 5, lines 47-55).

As per claim 12, the claim is rejected for the same reasons as cited in claim 4 above combined with Pekarich's disclosure of a computer program product in a computer readable recordable-type medium for processing instructions (Pekarich, col. 5, lines 47-55).

As per claim 16, the claim is rejected for the same reasons as cited in claim 8 above combined with Pekarich's disclosure of a computer program product in a computer readable recordable-type medium for processing instructions (Pekarich, col. 5, lines 47-55).

As per claim 17, Pekarich discloses an apparatus for processing instructions comprising:

means for receiving a threshold value and an identification of a plurality of addresses to be monitored during the execution of a computer program (col. 4, lines 61-63; col. 3, lines 7-12; col. 1, lines 32-42); *It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer.*

Pekarich does not expressly disclose means for associating hardware counters with the plurality of addresses;

means for executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered;

and means for performing an action in response to a determination that a predefined relationship between the threshold value and a combination of values obtained from the hardware counters is present.

IBMTD discloses means for associating hardware counters with the plurality of addresses (pg. 1, paragraph 3, lines 1-2); *It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer. Also, please see the citation note for the similar limitation in claim 1 above.*

and means for performing an action in response to a determination that a predefined relationship between the threshold value and a combination of values obtained from the hardware counters is present (pg. 1, paragraph 5, lines 8-10). *It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer. Also, please see the citation note for the similar limitation in claim 1 above.*

Pekarich and IBMTD are analogous art because they are from the same field of endeavor, that being memory management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement IBMTD's PFT and hardware counters with Pekarich's address range table.

The motivation for doing so would have been to reduce the expense of operations by allowing more immediate and more cost-effective memory management with the use of a hardware cycle counter and PFT cycle counter (IBMTD, pg. 1, paragraph 4, lines 5-7).

The combination of Pekarich/IBMTD does not expressly disclose means for executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered.

Burrows discloses means for executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered (col. 5, lines 13-17 and 31-34; Fig. 5, elements 520 and 540). *It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer. Also, please see the citation note for the similar limitation in claim 1 above.*

The combination of Pekarich/IBMTD and Burrows are analogous art because they are from the same field of endeavor, that being data processing systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Burrow's dynamic determination of hint field values within Pekarich/IBMTD's address range table.

The motivation for doing so would have been to measurably improve system performance by making code run faster (Burrows, col. 6, lines 16-20).

Therefore, it would have been obvious to combine Pekarich, IBMTD, and Burrows for the benefit of obtaining the invention as specified in claim 17.

As per claim 18, the combination of Pekarich/IBMTD/Burrows discloses means for arithmetically combining values of the hardware counters to generate a combined counter value (IBMTD, pg. 1, paragraph 5, line 8); *It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer. Also, please see the citation note for the similar limitation in claim 2 above.*

means for comparing the combined counter value to the threshold value (IBMTD, pg. 1, paragraph 5, lines 8-9); *It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer.*

and means for performing the action in response to a relationship between the combined counter value and the threshold value being present (IBMTD, pg. 1, paragraph 5, lines 9-10). *It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer.*

As per claim 20, the combination of Pekarich/IBMTD/Burrows discloses means for arithmetically combining values of the hardware counters, means for comparing the combined counter value to the threshold value, and means for performing the action operate in response to incrementing a counter (Pekarich, col. 5, lines 17-23). *It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer. Also, please see the citation note for claim 4 above.*

As per claim 23, the combination of Pekarich/IBMTD/Burrows discloses means for arithmetically combining values of the hardware counters includes combining values in accordance with a condition indicated by a performance monitoring application (IBMTD, pg. 1, paragraph 5, line 8). *It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer. Also, please see the citation note for claim 8 above.*

Claims 3, 6, 11, 14, 19, and 21 are rejected under 35 U.S.C. 103(a) as being obvious over Pekarich in view of IBMTD and in further view of Burrows as applied to claims 1, 9, and 17 above, and in even further view of Levine et al. (U.S. Patent 5,797,019).

As per claim 3, the combination of Pekarich/IBMTD/Burrows discloses a relationship between the combined counter value and the threshold value (IBMTD, pg. 1, paragraph 5, lines 8-9).

The combination of Pekarich/IBMTD/Burrows does not expressly disclose generating an interrupt if the predetermined relationship between the combined counter value and the threshold value is present.

Levine discloses generating an interrupt if the predetermined relationship between the counter value and the threshold value is present (col. 11, lines 3-7).

The combination of Pekarich/IBMTD/Burrows and Levine are analogous art because they are from the same field of endeavor, that being processing systems with counters.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Levine's threshold invoked interrupt with Pekarich/IBMTD/Burrows' combined counter value system.

The motivation for doing so would have been to gain the benefit of having the performance monitor facility readily suitable for use in identifying system performance problems through use of appropriate counter values (Levine, col. 11, lines 7-9).

Therefore, it would have been obvious to combine Pekarich/IBMTD/Burrows and Levine for the benefit of obtaining the invention as specified in claim 3.

As per claim 6, the combination of Pekarich/IBMTD/Burrows/Levine discloses sending the interrupt to an interrupt handler of a performance monitoring application, wherein the interrupt handler performs an operation based on receipt of the interrupt (Levine, col. 9, lines 30-42; Fig. 4, elements 50, 57, 71, 77, and 79). *It should be noted that "performance monitor (PM)" is analogous to "performance monitoring application"*

and that "interrupt handling routines" are analogous to "operation based on receipt of the interrupt."

As per claim 11, the claim is rejected for the same reasons as cited in claim 3 above combined with Pekarich's disclosure of a computer program product in a computer readable recordable-type medium for processing instructions (Pekarich, col. 5, lines 47-55).

As per claim 14, the claim is rejected for the same reasons as cited in claim 6 above combined with Pekarich's disclosure of a computer program product in a computer readable recordable-type medium for processing instructions (Pekarich, col. 5, lines 47-55).

As per claim 19, the combination of Pekarich/IBMTD/Burrows discloses a relationship between the combined counter value and the threshold value (IBMTD, pg. 1, paragraph 5, lines 8-9).

The combination of Pekarich/IBMTD/Burrows does not expressly disclose generating an interrupt if the predetermined relationship between the combined counter value and the threshold value is present.

Levine discloses generating an interrupt if the predetermined relationship between the counter value and the threshold value is present (col. 11, lines 3-7).

The combination of Pekarich/IBMTD/Burrows and Levine are analogous art because they are from the same field of endeavor, that being processing systems with counters.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Levine's threshold invoked interrupt with Pekarich/IBMTD/Burrow's combined counter value system.

The motivation for doing so would have been to gain the benefit of having the performance monitor facility readily suitable for use in identifying system performance problems through use of appropriate counter values (Levine, col. 11, lines 7-9).

Therefore, it would have been obvious to combine Pekarich/IBMTD/Burrows and Levine for the benefit of obtaining the invention as specified in claim 19.

As per claim 21, the combination of Pekarich/IBMTD/Burrows/Levine discloses means for sending the interrupt to an interrupt handler of a performance monitoring application, wherein the interrupt handler performs an operation based on receipt of the interrupt (Levine, col. 9, lines 30-42; Fig. 4, elements 50, 57, 71, 77, and 79). *It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer. Also, please see the citation note for claim 6 above.*

Claims 7, 15, and 22 are rejected under 35 U.S.C. 103(a) as being obvious over Pekarich in view of IBMTD, in further view of Burrows, and in view even

further of Levine as applied to claims 3, 11, and 19 above, and in even further view of Bartfai et al. (U.S. Patent Application Publication 2003/0101367).

As per claim 7, the combination of Pekarich/IBMTD/Burrows/Levine disclose all the limitations of claim 7 except the operation is at least one of generating a log entry in a performance monitoring application log and notifying a log daemon process of an event.

Bartfai discloses the operation is at least one of generating a log entry in a performance monitoring application log and notifying a log daemon process of an event (paragraph 0030, lines 42-45; paragraph 0007, lines 20-22; paragraph 0037, lines 9-14; Fig. 2, element 140). *It should be noted that "Fault Service Daemon" is analogous to "log daemon."*

The combination of Pekarich/IBMTD/Burrows/Levine and Bartfai are analogous art because they are from the same field of endeavor, that being interrupt handling.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Bartfai's interrupt logging within Pekarich/IBMTD/Burrows/Levine's interrupt handling system based on combined counter values.

The motivation for doing so would have been to provide a mechanism for a more complete analysis of adapter error causes (Bartfai, paragraph 00300, lines 46-47).

Therefore, it would have been obvious to combine Pekarich/IBMTD/Burrows/Levine and Bartfai for the benefit of obtaining the invention as specified in claim 7.

As per claim 15, the claim is rejected for the same reasons as cited in claim 7 above combined with Pekarich's disclosure of a computer program product in a computer readable recordable-type medium for processing instructions (Pekarich, col. 5, lines 47-55).

As per claim 22, the combination of Pekarich/IBMTD/Burrows/Levine disclose all the limitations of claim 22 except the operation is at least one of generating a log entry in a performance monitoring application log and notifying a log daemon process of an event.

Bartfai discloses the operation is at least one of generating a log entry in a performance monitoring application log and notifying a log daemon process of an event (paragraph 0030, lines 42-45; paragraph 0007, lines 20-22; paragraph 0037, lines 9-14; Fig. 2, element 140). *It should be noted that "Fault Service Daemon" is analogous to "log daemon."*

The combination of Pekarich/IBMTD/Burrows/Levine and Bartfai are analogous art because they are from the same field of endeavor, that being interrupt handling.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Bartfai's interrupt logging within

Pekarich/IBMTD/Burrows/Levine's interrupt handling system based on combined counter values.

The motivation for doing so would have been to provide a mechanism for a more complete analysis of adapter error causes (Bartfai, paragraph 00300, lines 46-47).

Therefore, it would have been obvious to combine Pekarich/IBMTD/Burrows/Levine and Bartfai for the benefit of obtaining the invention as specified in claim 22.

Claims 5 and 13 are rejected under 35 U.S.C. 103(a) as being obvious over Pekarich in view of IBMTD, and in further Burrows as applied to claims 1 and 9 above, and in even further view of Randall Hyde, "The Art of Assembly Language," hereafter "Hyde."

As per claim 5, the combination of Pekarich/IBMTD/Burrows disclose arithmetically combining values of the counters (IBMTD, pg. 1, paragraph 5, line 8), comparing the combined counter value (IBMTD, pg. 1, paragraph 5, lines 8-9), and performing the action (IBMTD, pg. 1, paragraph 5, lines 9-10).

The combination of Pekarich/IBMTD/Burrows does not expressly disclose arithmetically combining values of the counters, comparing the combined counter value, and performing the action are performed within microcode of a processor of the data processing system.

Hyde discloses microcode of a processor of a data processing system (pg. 247, section 4.5, 2nd paragraph, lines 2-4).

The combination of Pekarich/IBMTD/Burrows and Hyde are analogous art because they are from the same field of endeavor, that being computer system design.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Hyde's microcode within Pekarich/IBMTD/Burrows' combined counter value system.

The motivation for doing so would have been to make better reuse of existing silicon on a CPU by using microcode subroutines to implement many common operations (Hyde, pg. 248, section 4.5, 6th paragraph, lines 1-4). Another motivation for doing so would have been to let programmers create some very complex instructions that consist of several different operations, thus providing programmers (especially assembly language programmers) with the ability to do more work with fewer instructions in their programs. In theory, this lets them write faster programs since they now execute half as many instructions, each doing twice the work of a simpler instruction set (Hyde, pg. 248, section 4.5, 7th paragraph, lines 1-4).

Therefore, it would have been obvious to combine Pekarich/IBMTD/Burrows and Hyde for the benefit of obtaining the invention as specified in claim 5.

As per claim 13, the claim is rejected for the same reasons as cited in claim 5 above combined with Pekarich's disclosure of a computer program product in a

computer readable recordable-type medium for processing instructions (Pekarich, col. 5, lines 47-55).

(10) Response to Arguments

Response to A.1. (Claims 1, 9, and 17)

Appellant argues on page 18 of the Appeal Brief that:

In contradistinction, the present invention in claim 1 provides an indicator that identifies the instruction as one that is to be monitored by a performance monitor unit.

The Examiner respectfully notes that the limitation "an indicator that identifies the instruction as one that is to be monitored by a performance monitor unit" is not recited in the language of claim 1. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Appellant argues on page 18 of the Appeal Brief that:

Therefore, Burrows does not teach or suggest executing the computer program and incrementing respective hardware counters ***when*** *the plurality of addresses are accessed* ***and a performance indicator associated with the plurality of addresses is encountered****, as recited in claim 1.*

The Examiner respectfully disagrees and refers Appellant to the portions of Burrows cited in the rejections of claims 1, 9, and 17 above. Appellants' "performance

indicator", when taking the broadest reasonable interpretation of the claim language, is merely an "indicator of action." As cited by Appellant on page 18 of the Appeal Brief, Burrows' hint fields help branch prediction logic of the CPU 190 to determine the address of the next instruction to be fetched. Thus, Burrows' hint field is an indicator of the next instruction to be fetched ("fetching" being an action). Accordingly, Burrows' hint field sufficiently discloses a "performance indicator."

For the sake of additional clarity the Examiner will now give a thorough explanation of how elements from the Burrows reference adequately disclose elements from the limitation in question. Firstly, it should be noted that because the Burrows reference is a computer implemented method, any action that occurs during operation, such as incrementing a counter, is accomplished via executing code in a computer program. In view of this fact, Burrows increments (i.e. executing a computer program and incrementing) the hit field (i.e. respective hardware counters) when there is a hit (i.e. addresses are accessed") and the best_hint field associated with the instructions (i.e. a performance indicator associated with the addresses) is accessed (i.e. encountered). It should be noted that the best_hint field is accessed in order for a determination to be made as to whether the current hint field is identical to the best_hint field. Accordingly, Burrows sufficiently discloses executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered.

Appellant argues on page 19 of the Appeal Brief that:

Consequently, Burrows teaches away from the present invention by counting every hint field...

The Examiner respectfully disagrees and refers Appellant to the portions of Burrows cited in the rejections of claims 1, 9, and 17 above. As is clearly shown in Burrows, col. 5, lines 31-24, Burrows only increments the hit field (i.e. counts) when the current hint field is identical to the best_hint field. Accordingly, Burrows does not count every hint field and therefore Burrows does not teach away from the present invention.

Appellant argues on page 19 of the Appeal Brief that:

....and Burrows does not teach or suggest executing the computer program and incrementing respective hardware counters ***when*** *the plurality of addresses are accessed* ***and a performance indicator associated with the plurality of addresses is encountered.***

The Examiner respectfully disagrees and refers Appellant above to the second section of the response to A.1. which details how Burrows discloses executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered. Accordingly, Burrows sufficiently discloses executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered.

Appellant argues on page 20 of the Appeal Brief that:

Since the references fail to teach or suggest executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed ***and a performance indicator associated with the plurality of addresses is encountered****, the Office Action has failed to establish a prima facie case of obviousness, because the Office Action does not show where each and every claim limitation is taught or fairly suggested by the applied prior art.*

The Examiner respectfully disagrees and refers Appellant above to the second section of the response to A.1. which details how Burrows discloses executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered. Accordingly, the Office action sufficiently established a prima facie case of obviousness.

Appellant argues on page 20 of the Appeal Brief that:

The applied references do not teach or suggest each and every claim limitation; therefore, Pekarich, IBMTD, and Burrows, taken alone or in combination, do not render claim 1 obvious. Independent claims 9 and 17 recite similar subject matter addressed above with respect to claim 1 and are allowable for similar reasons.

The Examiner respectfully disagrees and refers Appellant to the rejections of claims 1, 9, and 17 above, as well as the Examiner's responses to Appellants'

arguments directly above. Accordingly, the combination of Pekarich, IBMTD, and Burrows, renders claims 1, 9, and 17 obvious.

Appellant argues on page 20 of the Appeal Brief that:

Additionally, claims 2-8, 10-16, and 18-23 recite other additional combinations of features not taught or suggested by the references.

The Examiner respectfully disagrees and refers Appellant to the rejections of claims 2-8, 10-16, and 18-23 above. Accordingly, the references sufficiently disclose 2-8, 10-16, and 18-23.

Appellant argues on page 20 of the Appeal Brief that:

Furthermore, no suggestion is present in any of the references to modify the references to include such features. That is, there is no teaching or suggestion in Pekarich, IBMTD, and Burrows that a problem exists for which executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered, is a solution.

The Examiner respectfully notes that the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the

references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Appellant argues on page 20 of the Appeal Brief that:

Moreover, none of the reference teaches or suggests the desirability of incorporating the subject matter of the other reference. That is, there is no motivation offered in either reference for the alleged combination.

The Examiner respectfully disagrees and refers Appellant to the rejections of claims 1, 9, and 17 above and more specifically to the cited portions of the references themselves that contain the motivation to combine the references.

Appellant argues on page 21 of the Appeal Brief that:

None of the reference teaches or suggests executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered.

The Examiner respectfully disagrees and refers Appellant above to the second section of the response to A.1. which details how Burrows discloses executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered. Accordingly, the combination of Pekarich, IBMTD, and Burrows, sufficiently discloses executing the computer program and incrementing

respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered.

Appellant argues on page 21 of the Appeal Brief that:

Thus, the only teaching or suggestion to even attempt the alleged combination is based on a prior knowledge of Appellants' claimed invention thereby constituting impermissible hindsight reconstruction using Appellants' own disclosure as a guide.

The Examiner notes that in response to Appellants' argument that the Examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). As can been seen in the rejections above, when making the obviousness rejections the Examiner relied upon knowledge which was within the level of ordinary skill at the time the claimed invention was made, as well as knowledge gleaned from the references themselves (which is clear from the reference citations above). Accordingly, the reconstruction is proper.

Appellant argues on page 21 of the Appeal Brief that:

One of ordinary skill in the art, being presented only with Pekarich, IBMTD, and Burrows, and without having a prior knowledge of Appellants' claimed invention, would not have found it obvious to combine and modify Pekarich, IBMTD, and Burrows to arrive at Appellants' claimed invention, as recited in claim 1. To the contrary, even if one were somehow motivated to combine Pekarich, IBMTD, and Burrows, and it were somehow possible to combine the systems, the result would not be the invention, as recited in claim 1. The resulting system would still fail to execute the computer program and increment respective hardware counters when the plurality of addresses are accessed ***and*** *a performance indicator associated with the plurality of addresses is encountered.*

The Examiner respectfully disagrees and refers Appellant above to the second section of the response to A.1. which details how Burrows discloses executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered. Accordingly, the resulting system would succeed to execute the computer program and increment respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered.

Appellant argues on page 21 of the Appeal Brief that:

In view of the above, Appellants respectfully submit that the Pekarich, IBMTD, and Burrows, taken alone or in combination, fail to teach or suggest the features of claims 1, 9, and 17.

The Examiner respectfully disagrees and refers Appellant above to the second section of the response to A.1. which details how Burrows discloses executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered. Accordingly, the combination of Pekarich, IBMTD, and Burrows sufficiently discloses the features of claims 1, 9, and 17.

Response to A.2. (Claims 8, 16, and 23)

Appellant argues on page 22 of the Appeal Brief that:

With regard to claims 8, 16, and 23 in this group, Pekarich, IBMTD, and Burrows, taken alone or in combination, do not teach or suggest arithmetically combining values of the hardware counters includes combining values in accordance with a condition indicated by a performance monitoring application. ...Appellants are claiming that the values of the hardware counters are arithmetically combined when a condition indicated by a performance monitoring application is met. Appellants are not claiming a data structure for storing a difference in calculation as alleged by the Office Action. Thus, Pekarich and IBMTD, alone or in combination do not teach or suggest arithmetically combining values of the hardware counters includes combining values in accordance with a condition indicated by a performance monitoring application.

The Examiner respectfully disagrees and notes that the limitation "the values of the hardware counters are arithmetically combined when a condition indicated by a performance monitoring application is met" is not recited in the language of claims 8, 16, or 23. The Examiner asserts that the limitation "combining values when a condition is met" is very different from the limitation "combining values in accordance with a condition" as is stated in claims 8, 16, and 23. Thus, when taking the broadest reasonable interpretation of claims 8, 16, and 23 as stated, it is clear that IBMTD sufficiently discloses subtracting (i.e. arithmetically combining) values of the hardware counters includes combining values in accordance with the subtraction function of the ALU (i.e. a condition) indicated by commands from the CPU (i.e. a performance monitoring application). Accordingly, the combination of Pekarich, IBMTD, and Burrows sufficiently discloses arithmetically combining values of the hardware counters includes combining values in accordance with a condition indicated by a performance monitoring application.

Response to B. (Claims 3, 6, 11, 14, 19, and 21)

Appellant argues on page 23 of the Appeal Brief that:

In view of the above, Pekarich, IBMTD, Burrows, and Levine, taken either alone or in combination, fail to teach or suggest the specific features recited in independent claims 1, 9, and 17, from which claims 3, 6, 11, 14, 19, and 21 depend.

The Examiner respectfully disagrees and refers Appellant above to the second section of the response to A.1. which details how Burrows discloses executing the

computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered. Accordingly, the combination of Pekarich, IBMTD, Burrows, and Levine sufficiently discloses claims 3, 6, 11, 14, 19, and 21.

Response to V. (Claims 7, 15, 22)

Appellant argues on page 23 of the Appeal Brief that:

In view of the above, Pekarich, IBMTD, Burrows, Levine, and Bartfai, taken either alone or in combination, fail to teach or suggest the specific features recited in independent claims 1, 9, and 17, from which claims 7, 15, and 22 depend.

The Examiner respectfully disagrees and refers Appellant above to the second section of the response to A.1. which details how Burrows discloses executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered. Accordingly, the combination of Pekarich, IBMTD, Burrows, Levine, and Bartfai sufficiently discloses claims 7, 15, and 22.

Response to VI. (Claims 5 and 13)

In view of the above, Pekarich, IBMTD, Burrows, and Hyde, taken either alone or in combination, fail to teach or suggest the specific features recited in independent claims 1, 9, (sic) from which claims 5 and 13 depend.

The Examiner respectfully disagrees and refers Appellant above to the second section of the response to A.1. which details how Burrows discloses executing the computer program and incrementing respective hardware counters when the plurality of addresses are accessed and a performance indicator associated with the plurality of addresses is encountered. Accordingly, the combination of Pekarich, IBMTD, Burrows, and Hyde sufficiently discloses claims 5 and 13.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Arpan Savla

Conferees:

Sanjiv Shah

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Lynne H. Browne

Lynne H. Browne
Appeal Specialist, TQAS
Technology Center 2100